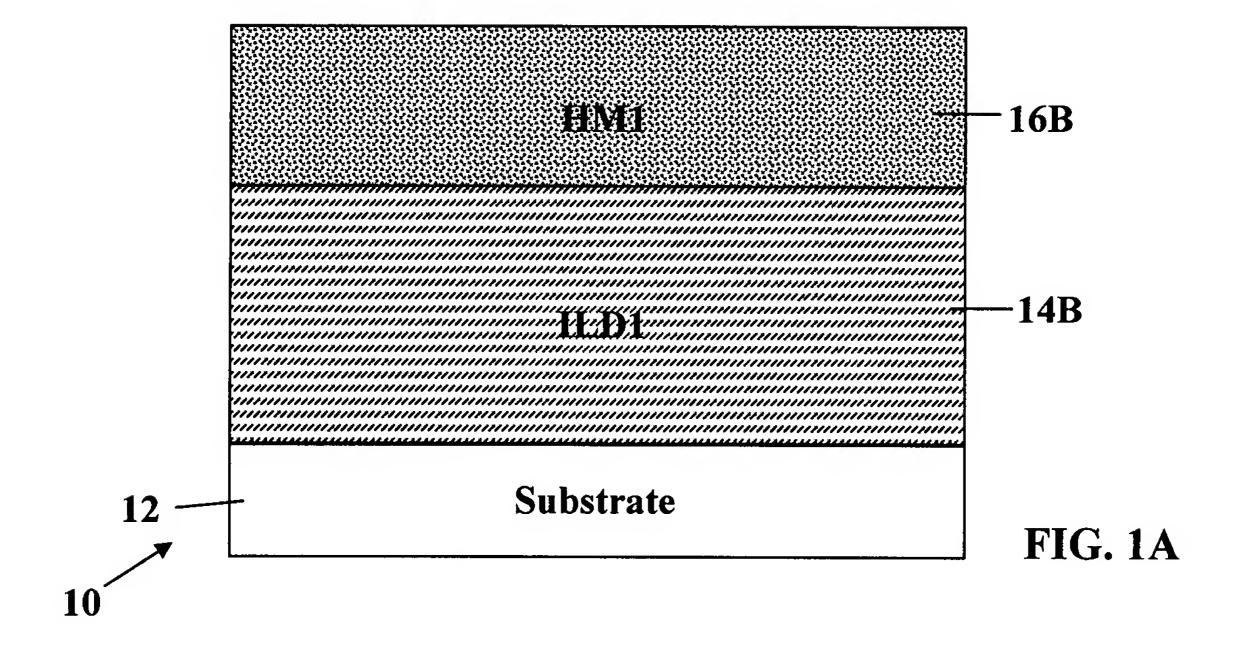
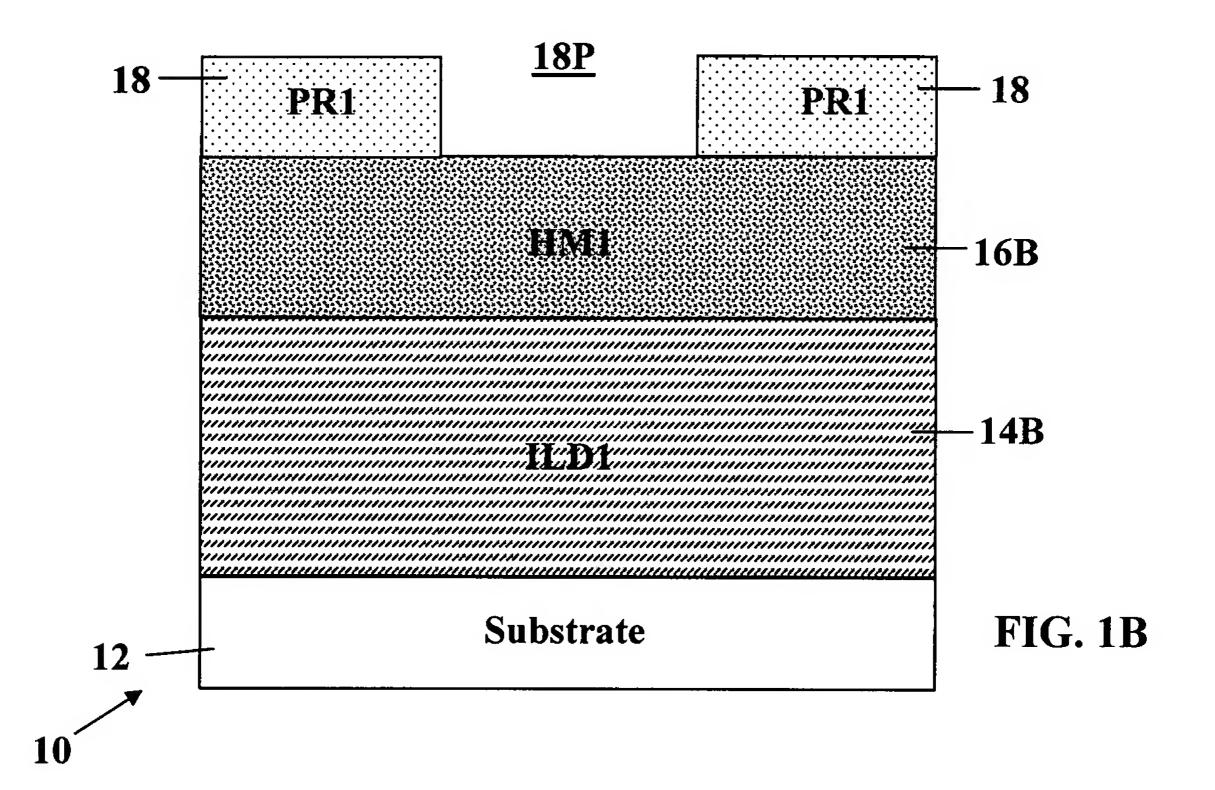
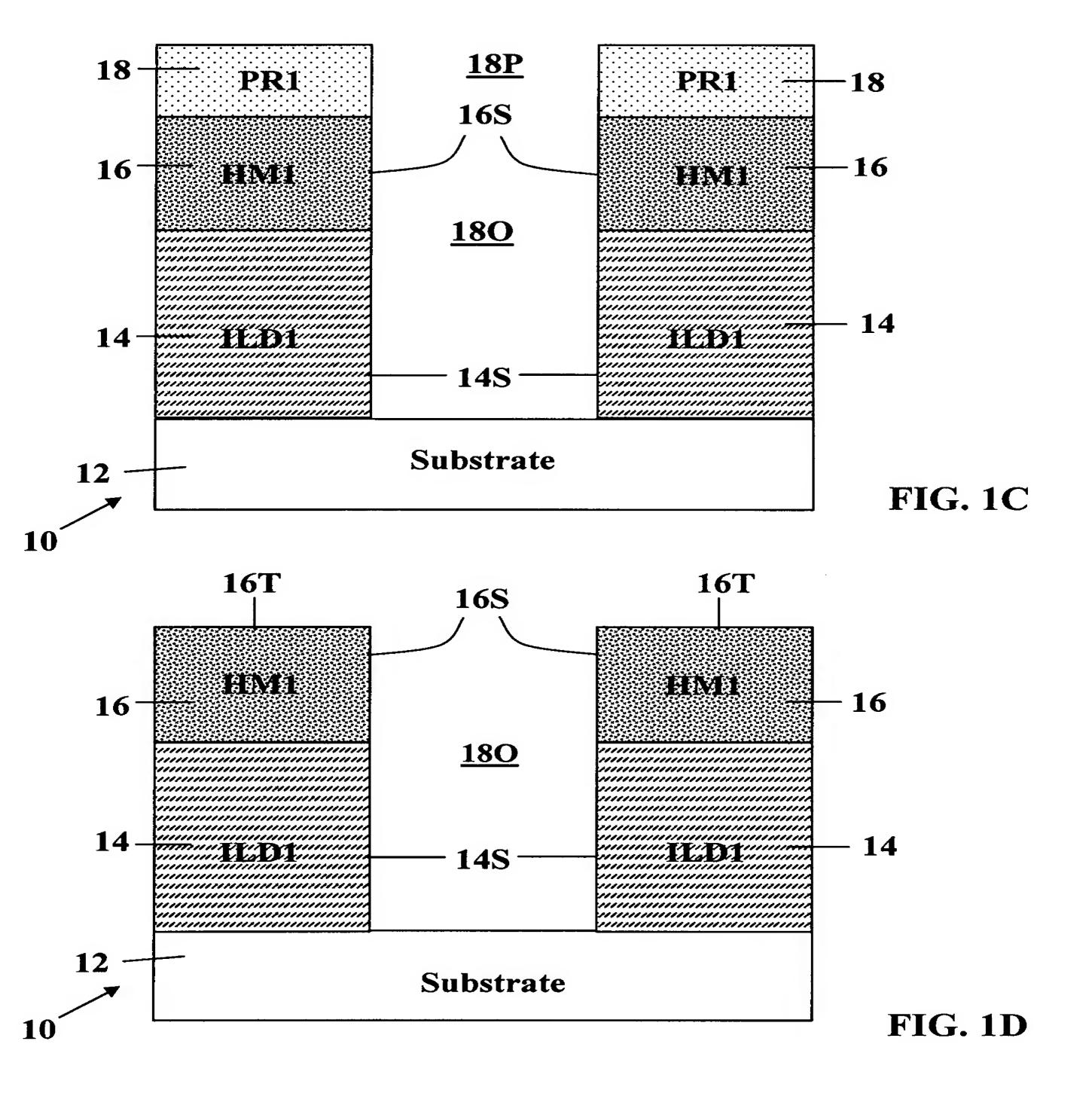
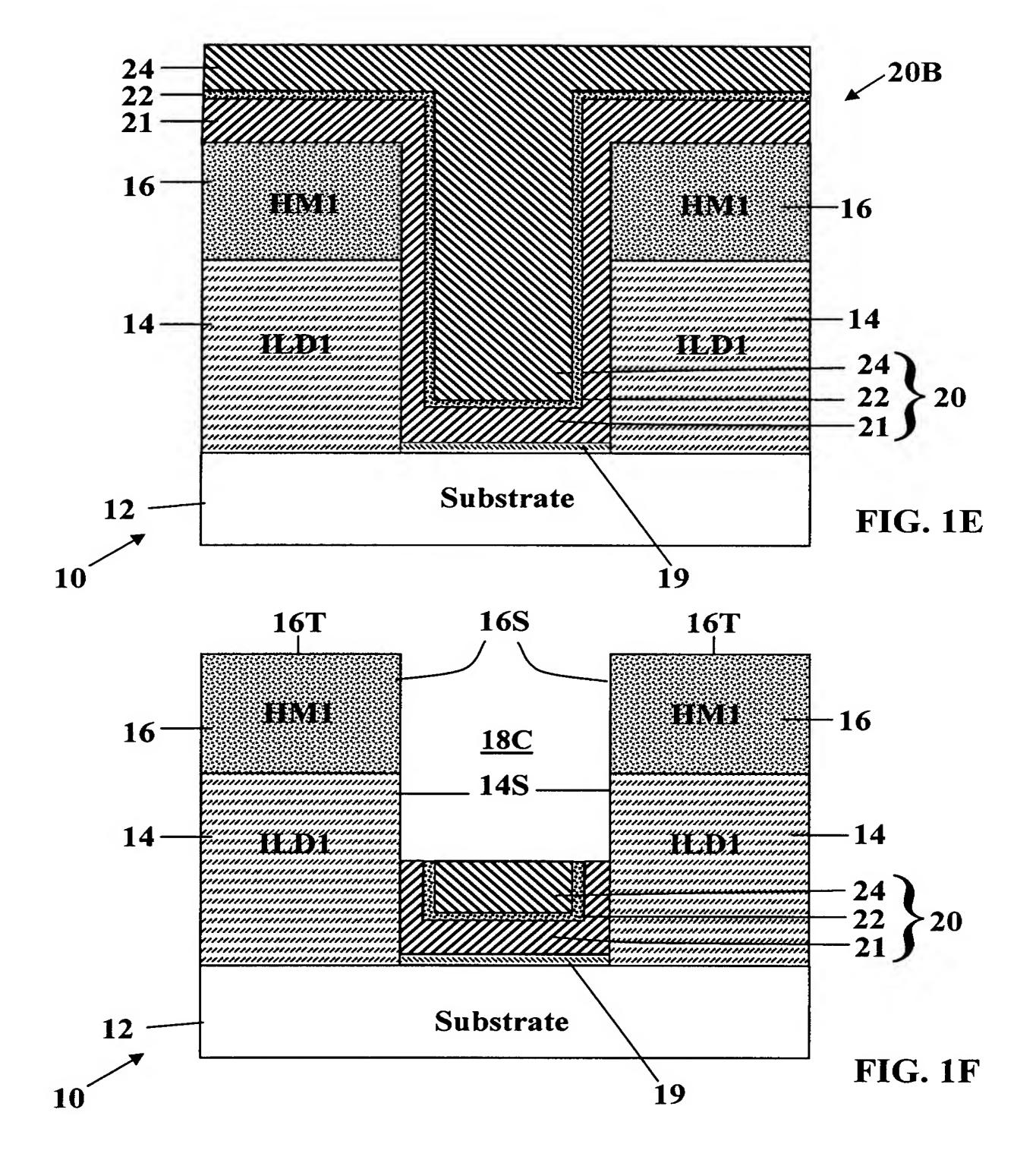
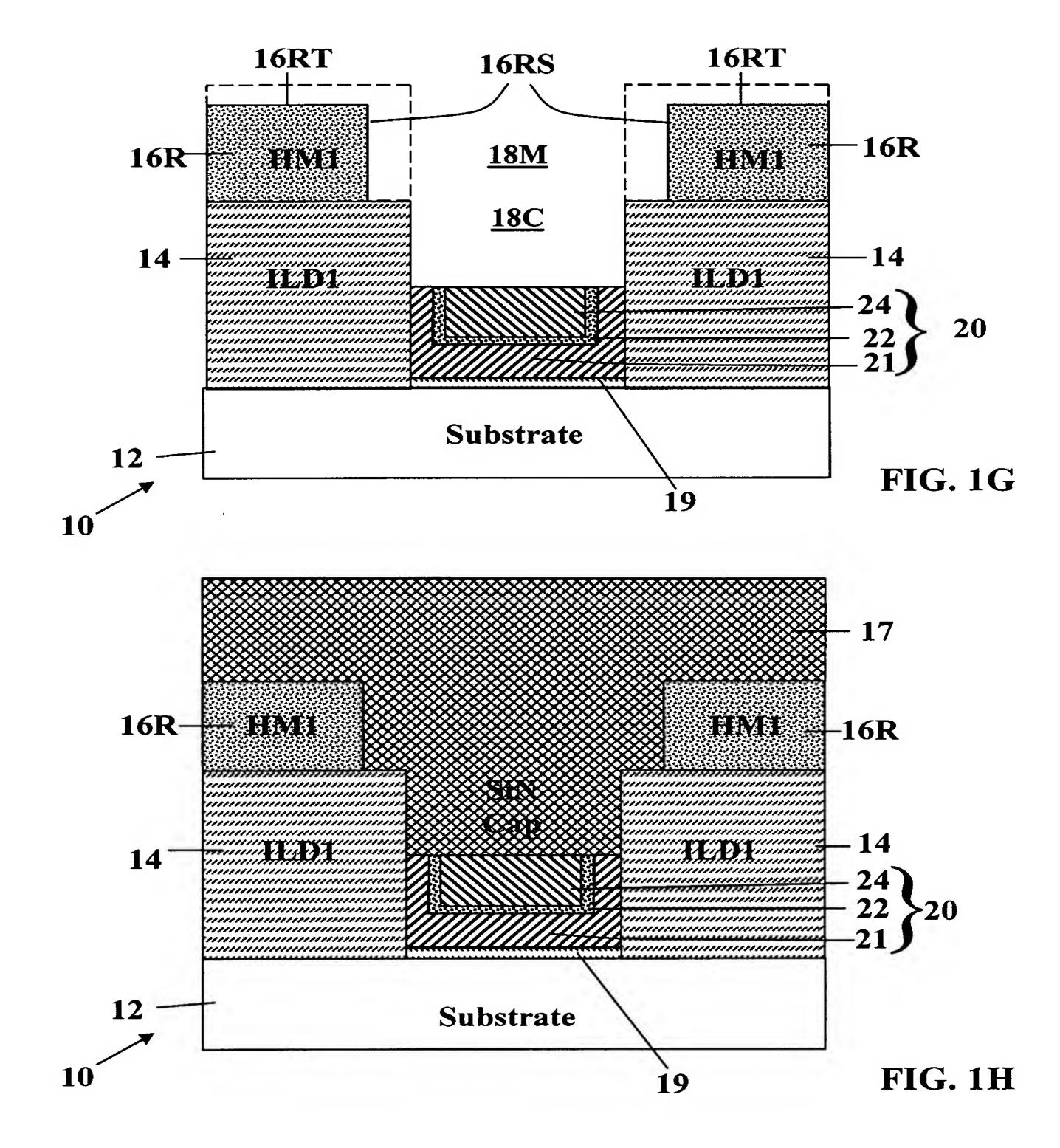
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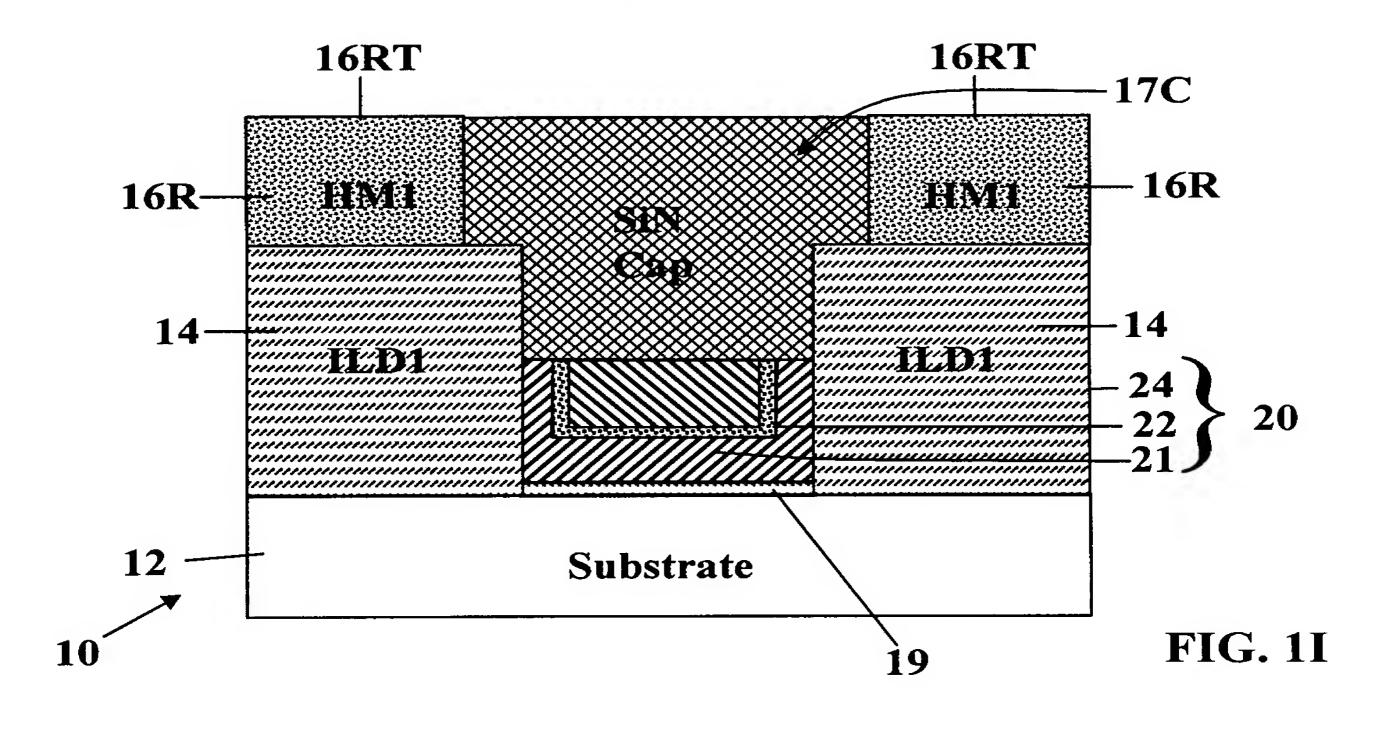


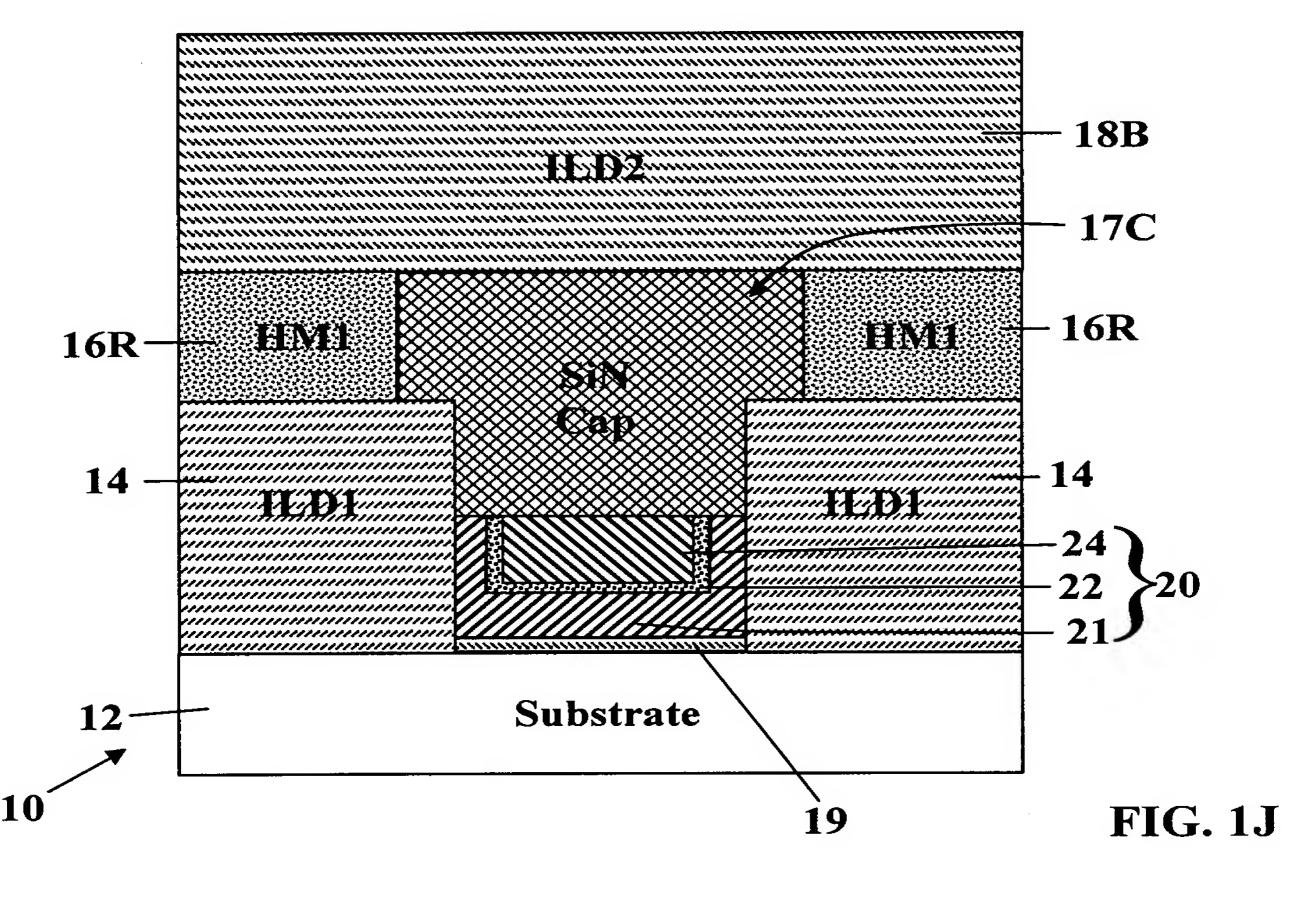


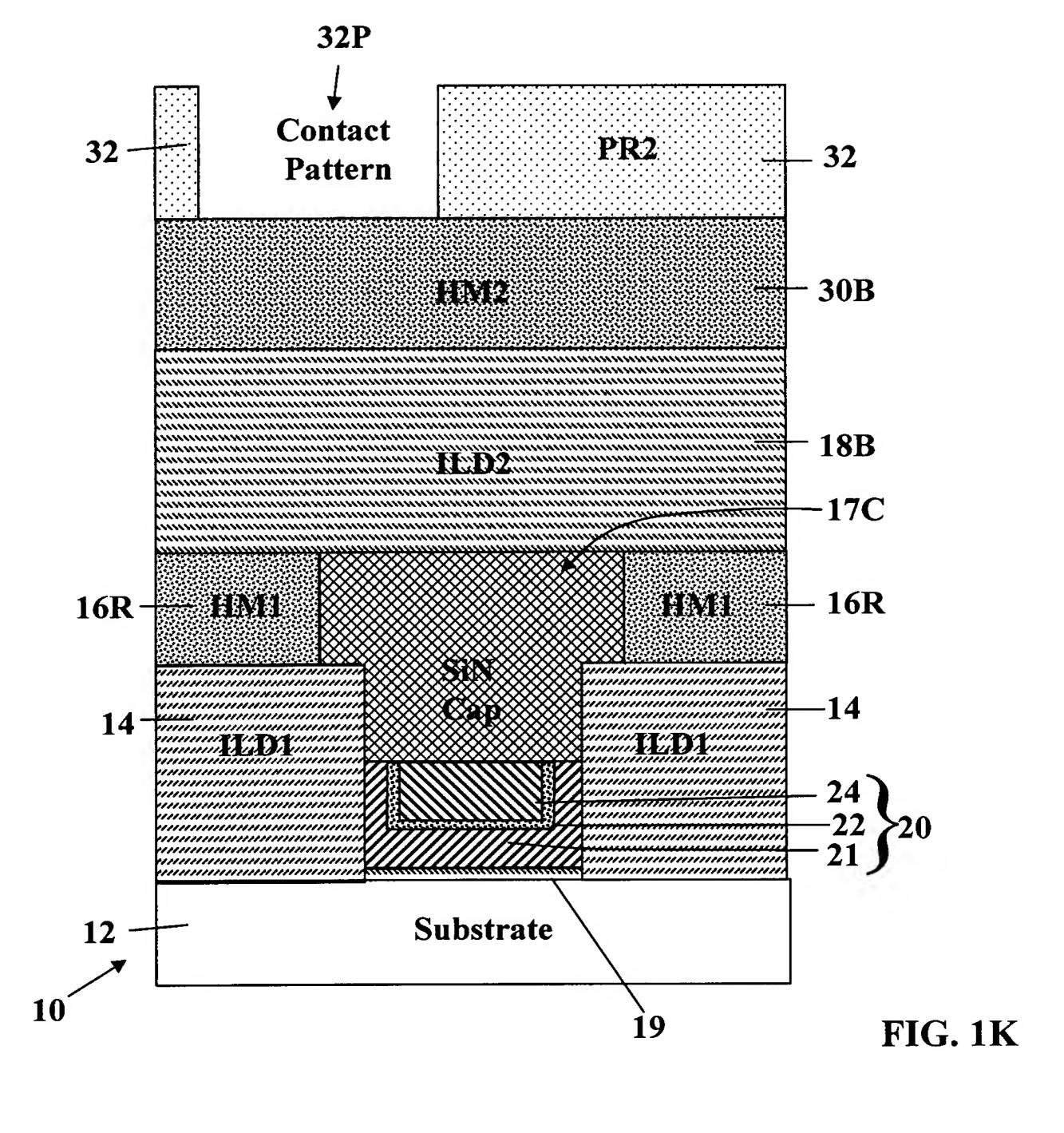




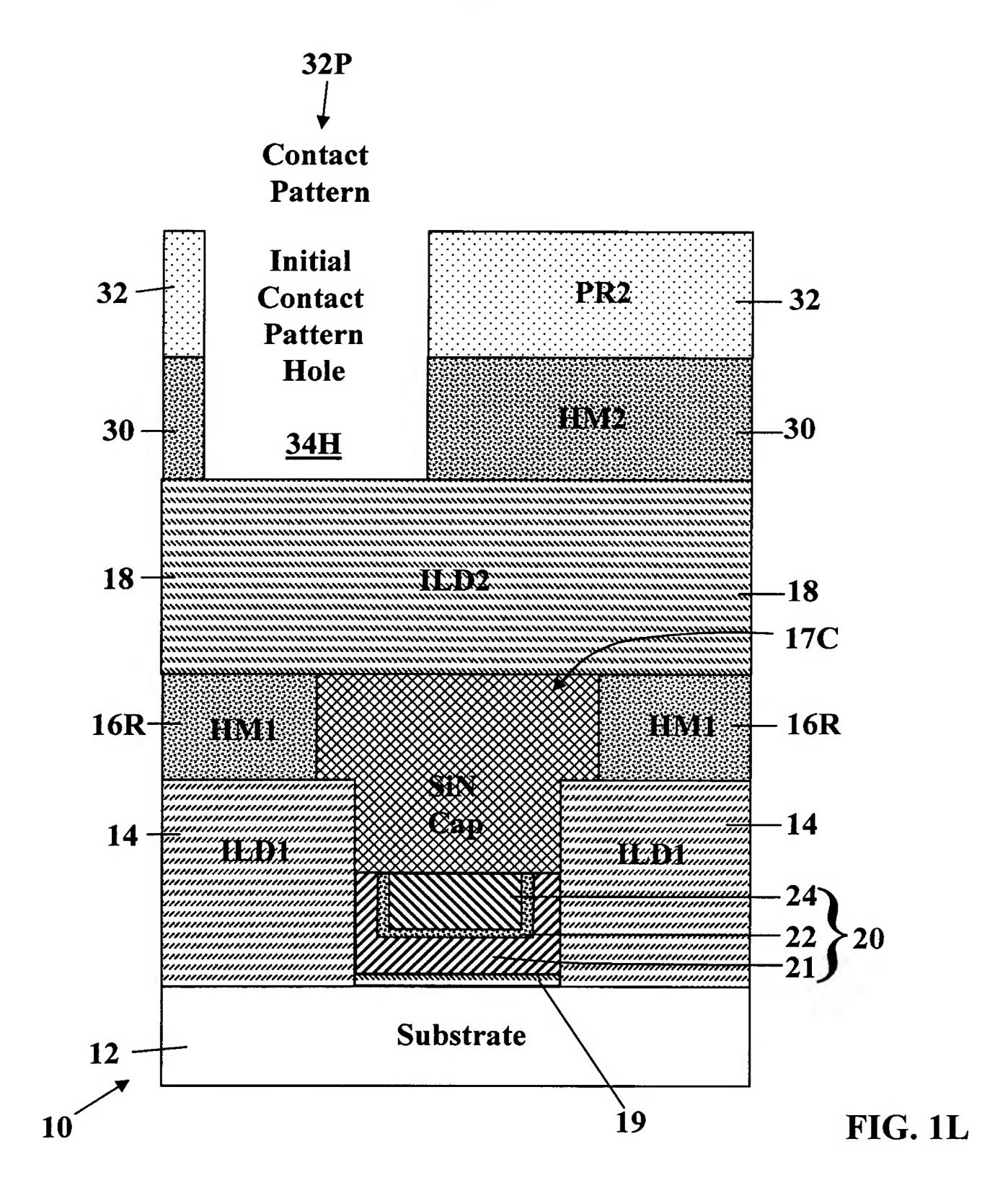
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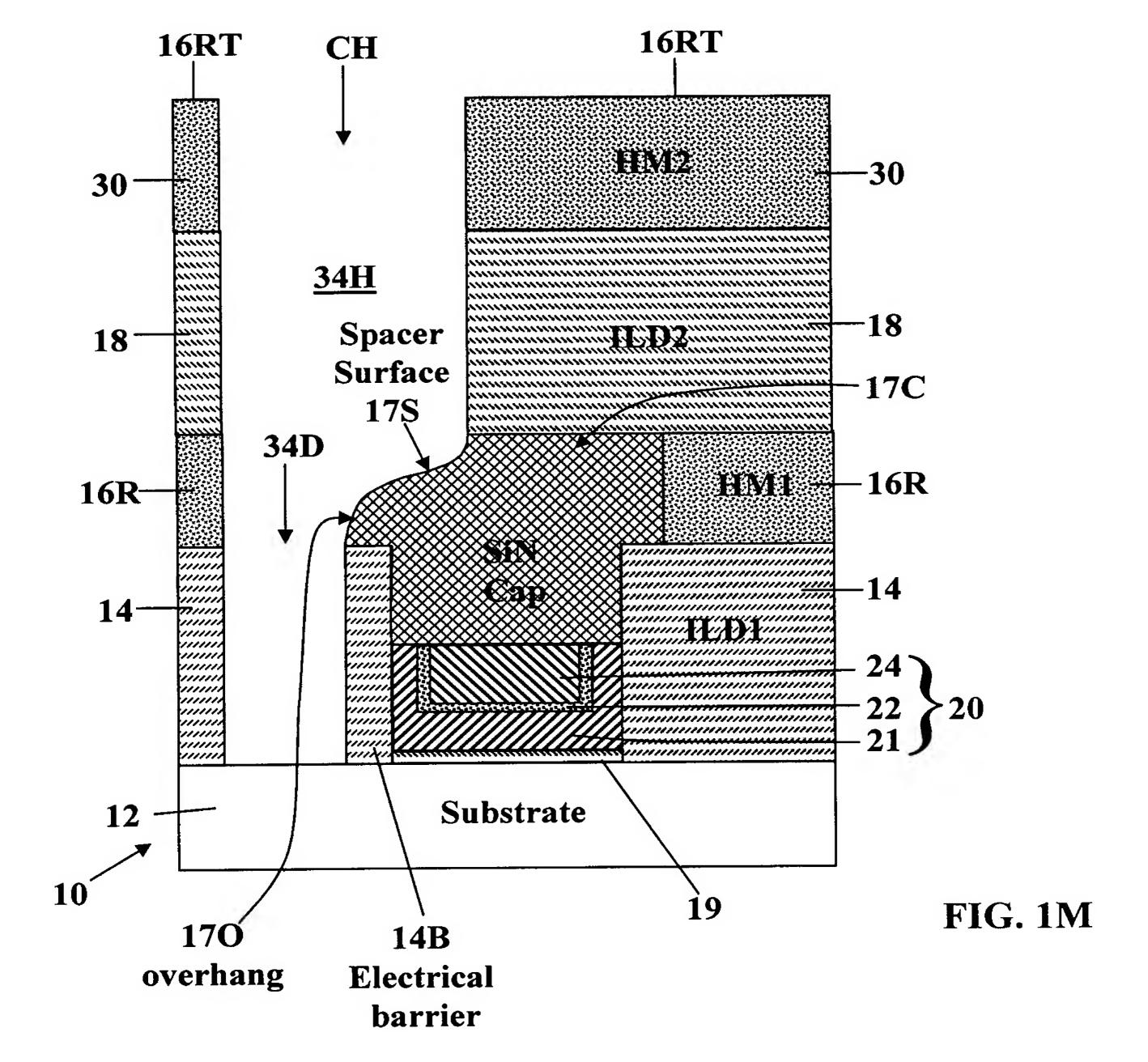


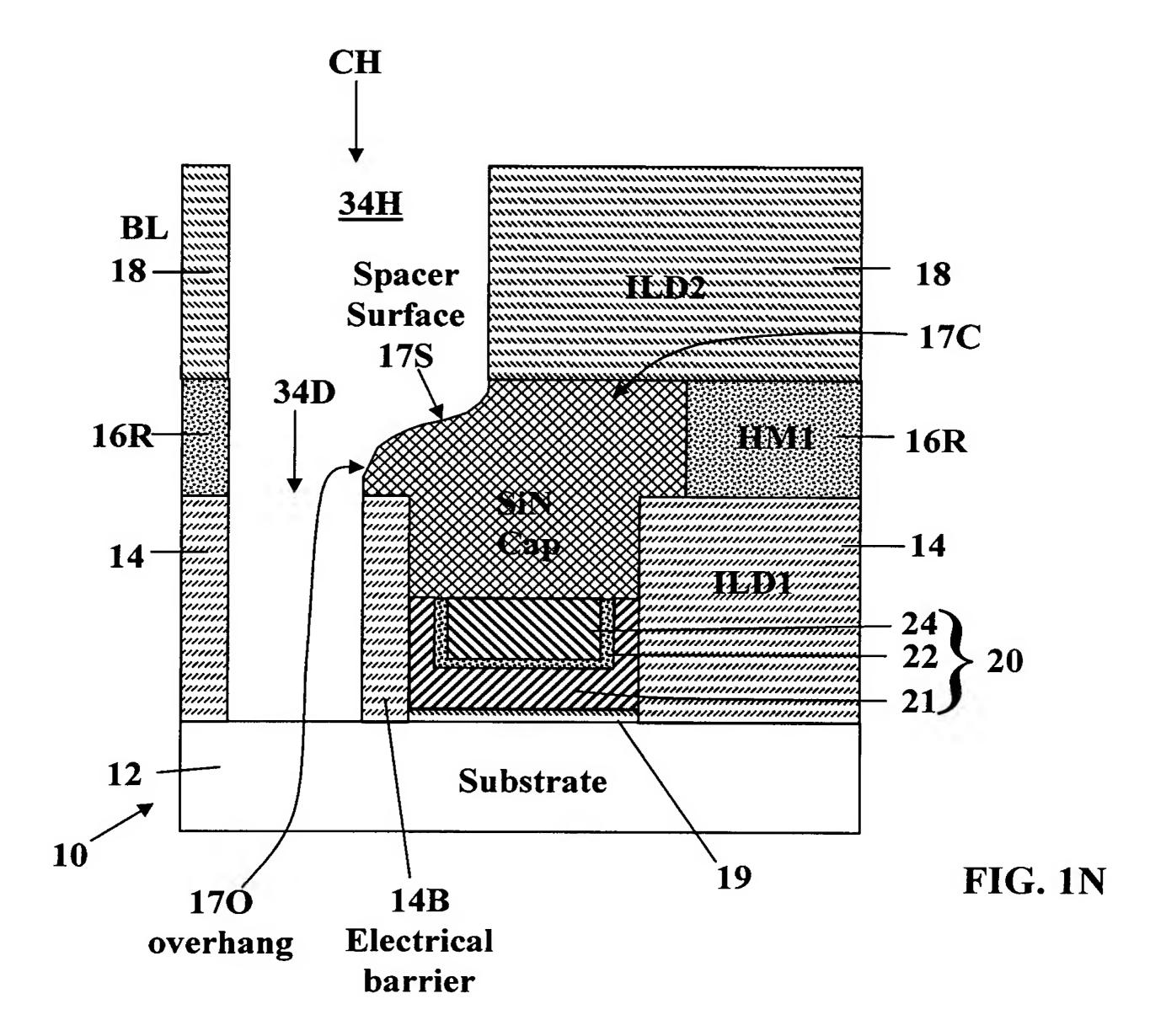


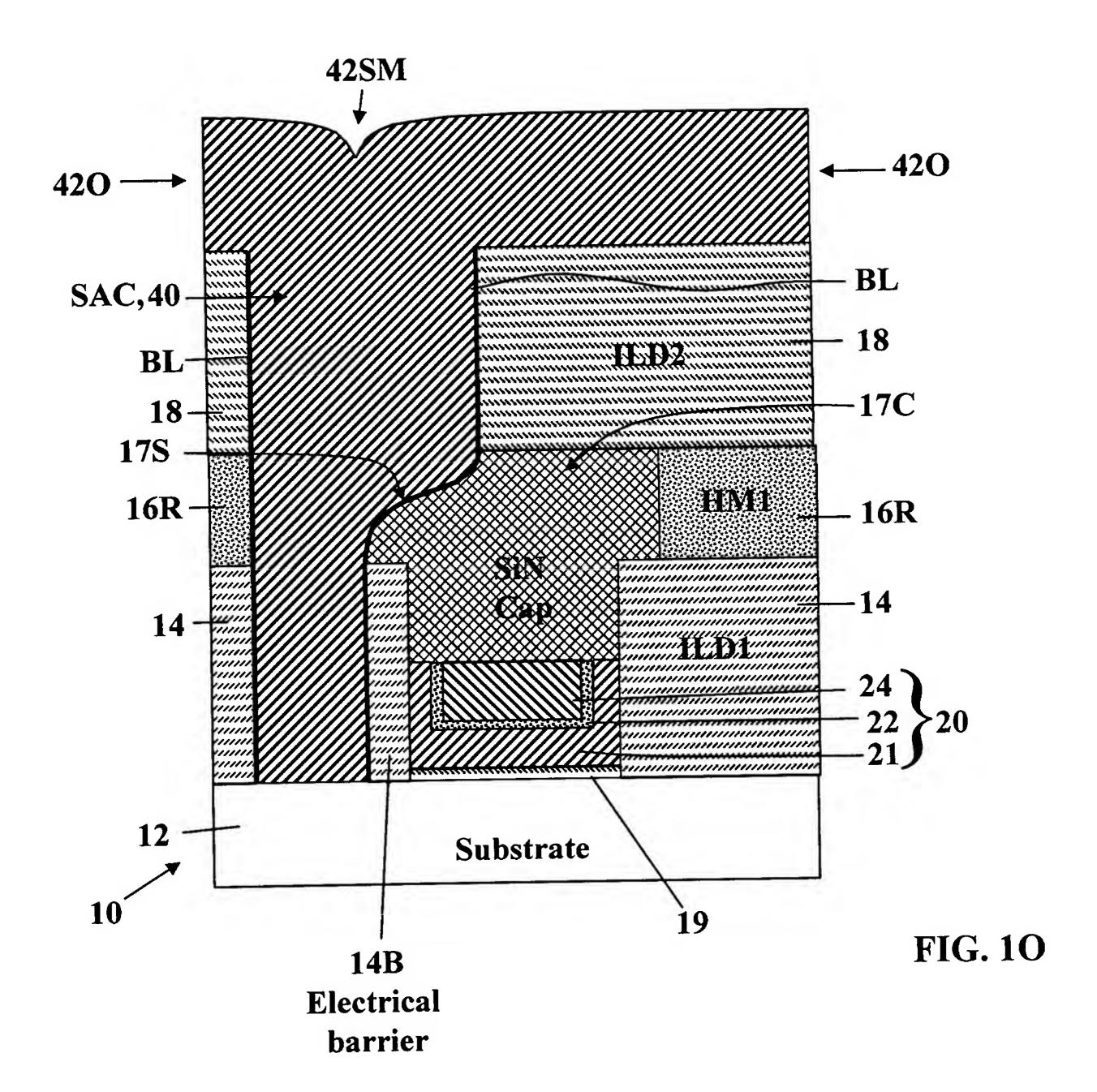


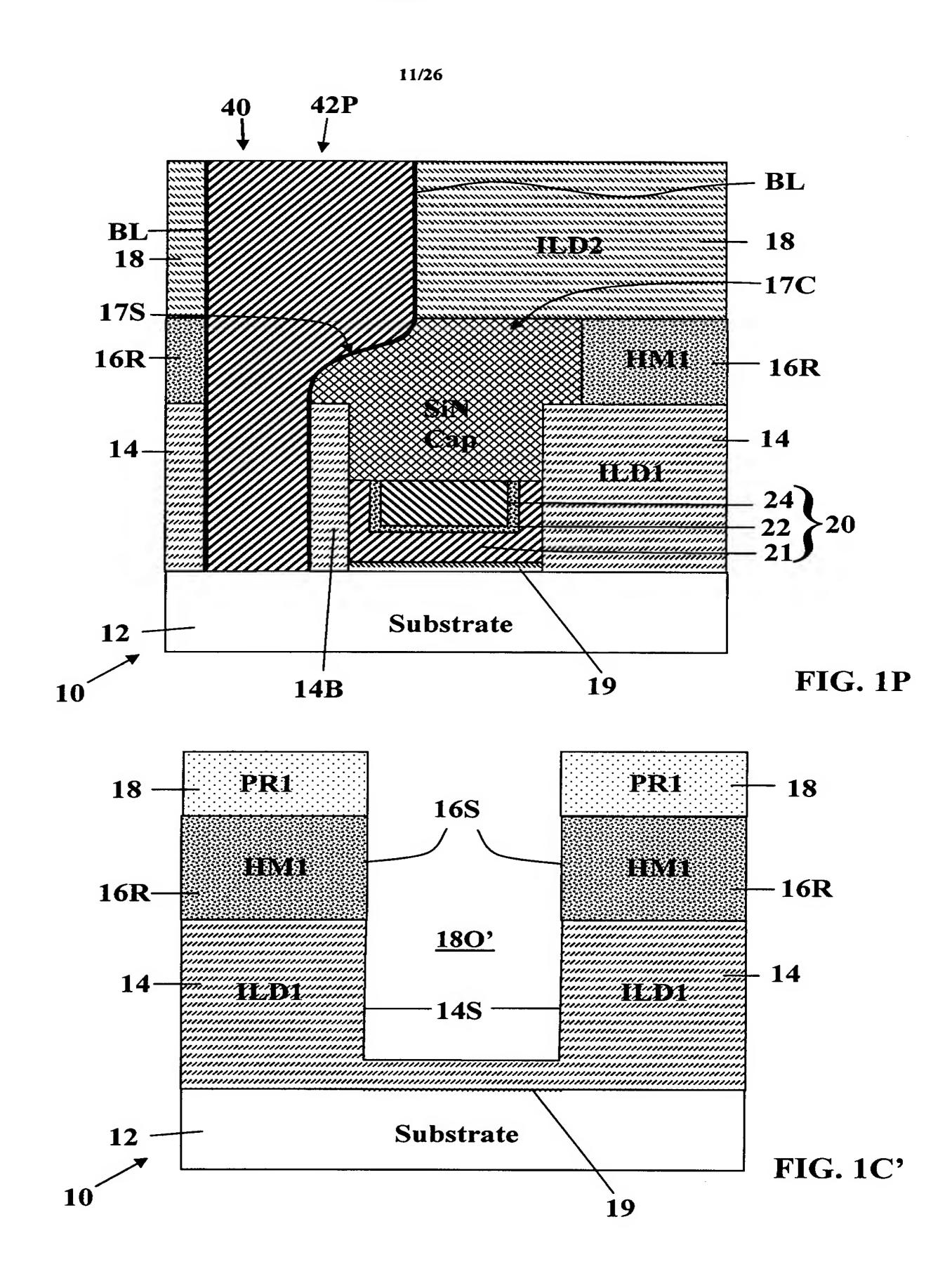
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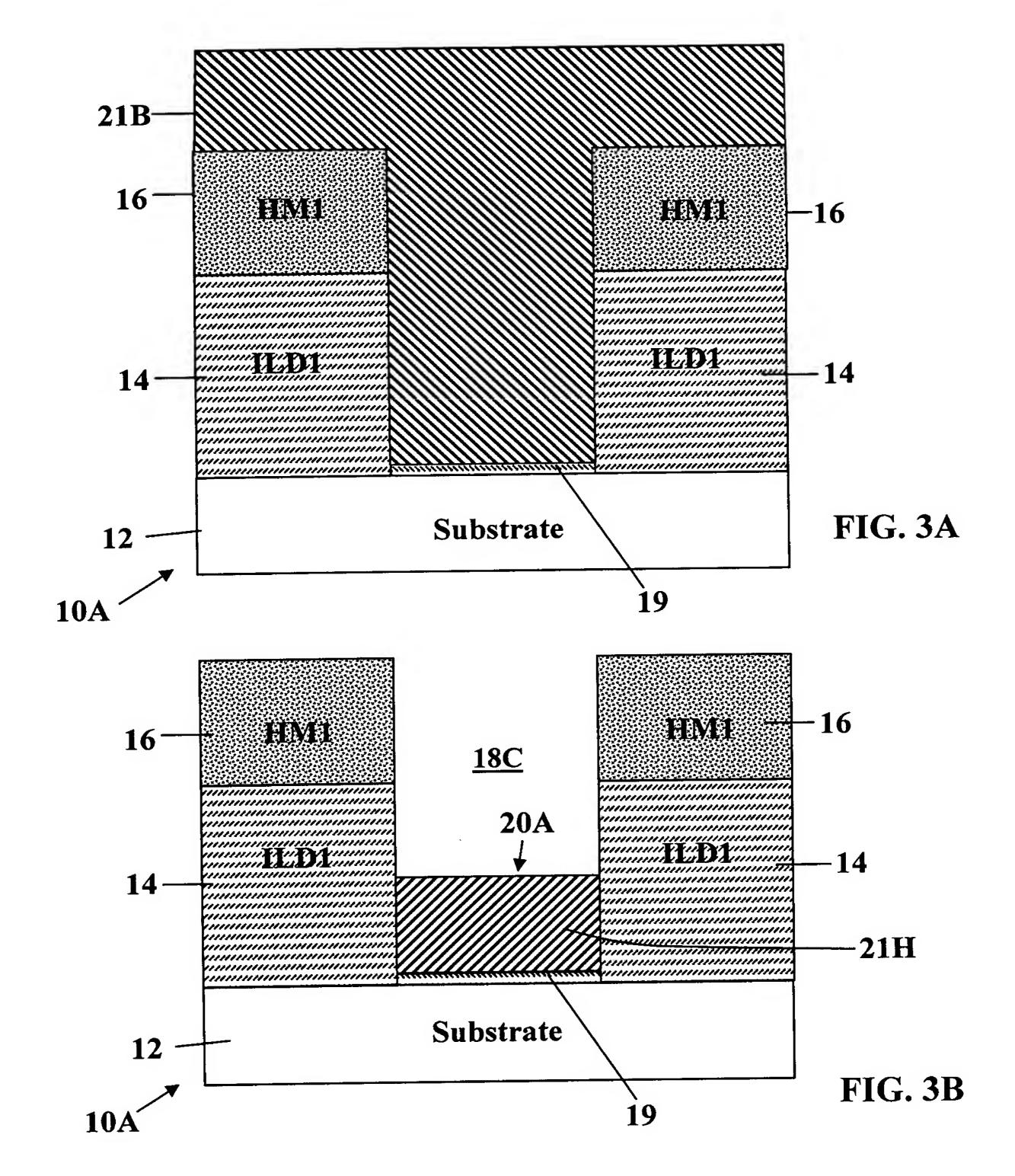




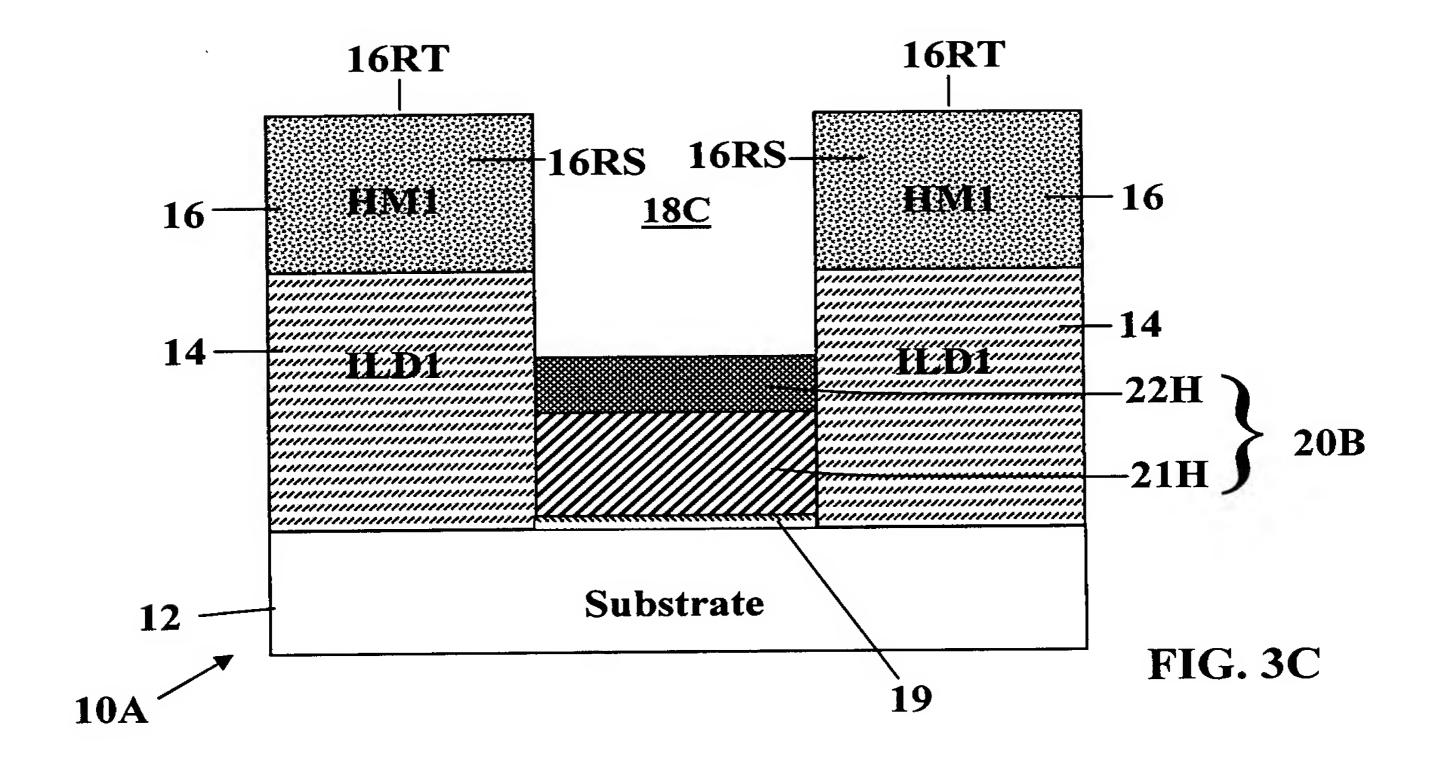


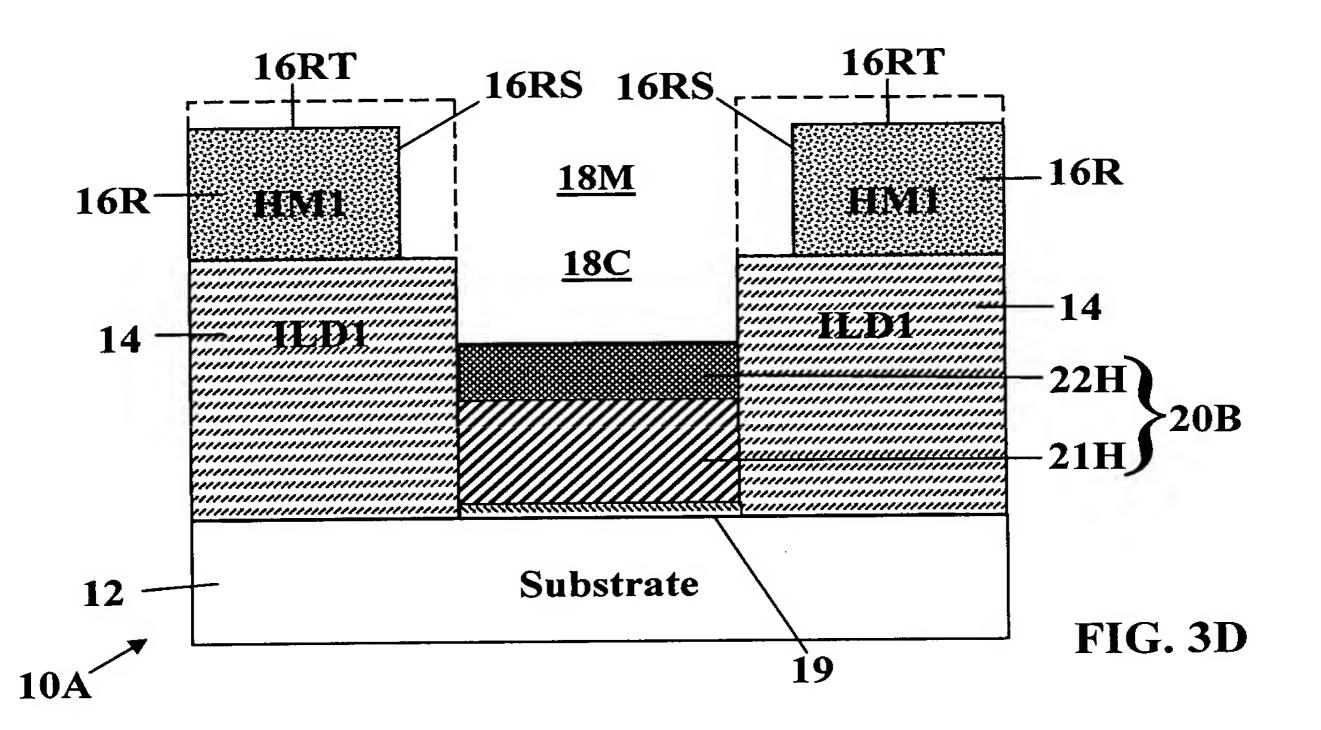


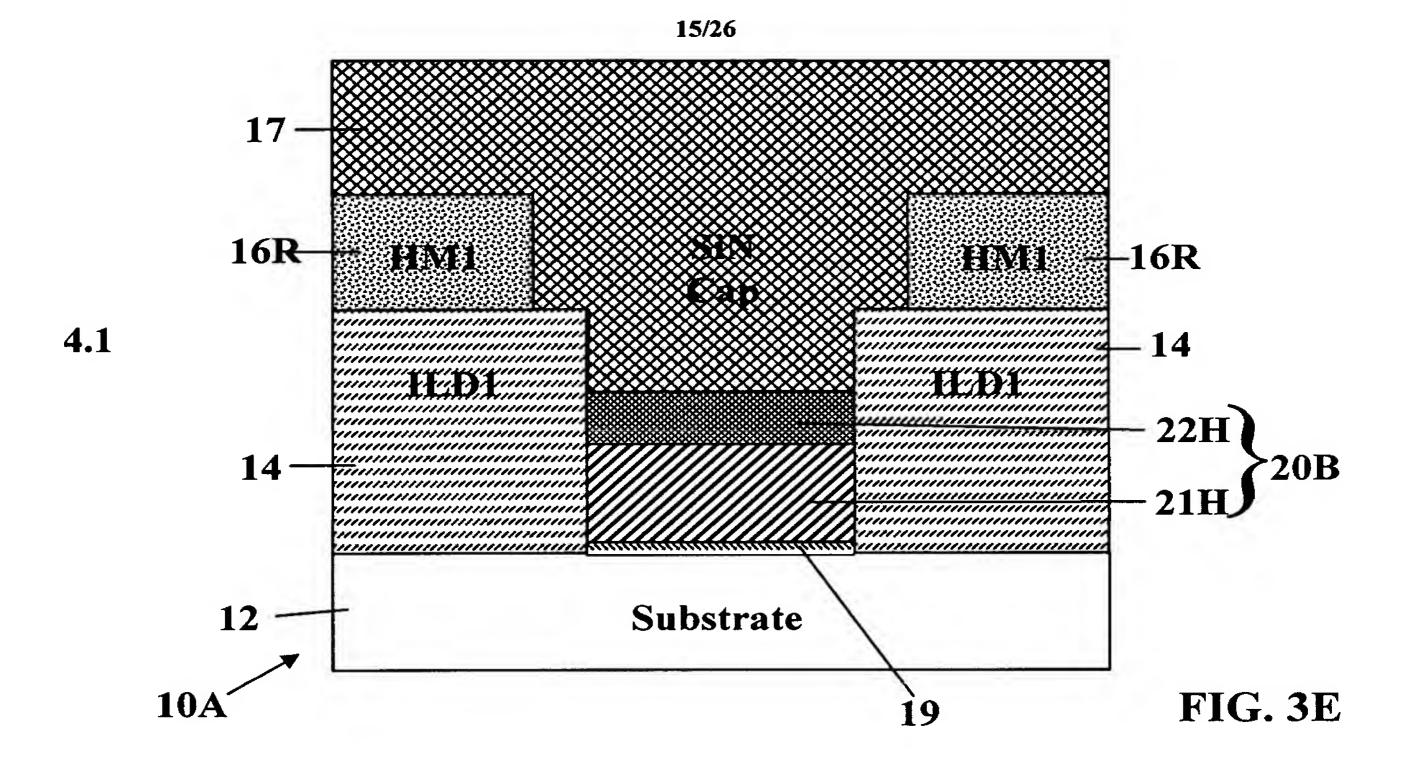
12/26 **START** - 50 · 51 DEPOSIT ILD1 LAYER AND HARD MASK 1 LAYER ON SUBSTRATE **52** FORM PATTERNED RESIST MASK 1 OVER HARD MASK 1 LAYER ETCH MASK 1 PATTERN THROUGH HARD MASK 1 LAYER AND ILD1 53 LAYER TO FORM A SLOT DOWN TO OR NEAR SUBSTRATE 54 STRIP RESIST AND FORM DIELECTRIC ON SUBSTRATE IN SLOT DEPOSIT LAMINATED DAMASCENE CONDUCTOR LAYERS 55 ONTO THE DEVICE AND INTO THE SLOT 56 ETCH TO RECESS THE DAMASCENE CONDUCTOR IN THE SLOT USE ISOTROPIC ETCH OF HARD MASK 1 TO WIDEN SLOT AT TOP - 57 **58 DEPOSIT BLANKET CAPPING LAYER** 59 PLANARIZE CAPPING LAYER TO EXPOSE TOP OF HARD MASK 60 DEPOSIT ILD2 LAYER AND HARD MASK 2 LAYER ON SUBSTRATE 61 FORM PATTERNED RESIST MASK 2 OVER HARD MASK 2 LAYER ETCH MASK 2 PATTERN THROUGH HARD MASK 2 LAYER AND ILD2 **62** LAYER TO FORM INITIAL CONTACT HOLE PATTERN; STRIP RESIST ETCH SAC CONTACT HOLE THROUGH ILD2, HARD MASK 2 AND ILD1 63 TO SUBSTRATE AND PATTERN SPACER/OVERHANG OF CAP 64 **STRIP HARD MASK 2** DEPOSIT CONTACT MATERIAL IN CONTACT HOLE AND PLANARIZE 65 FIG. 2 66 **END**

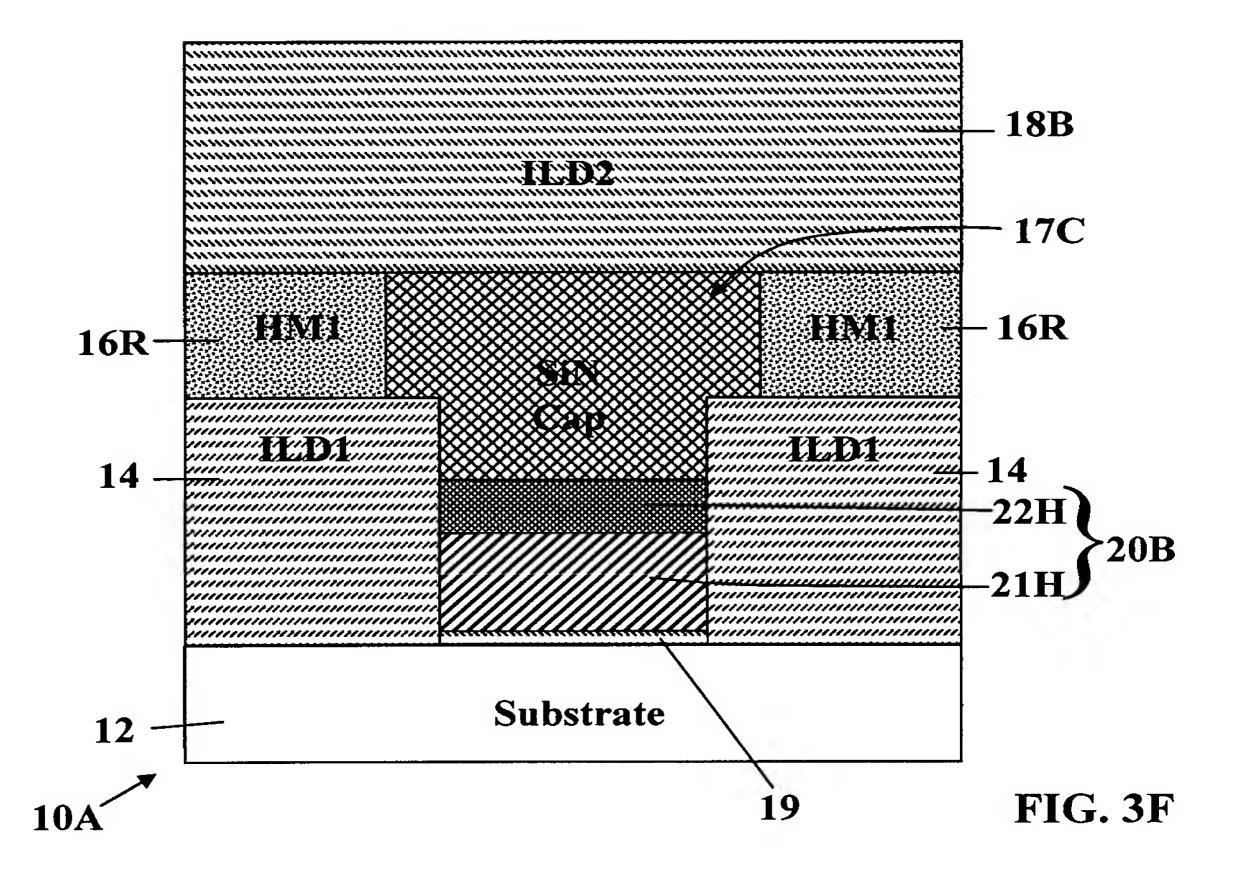


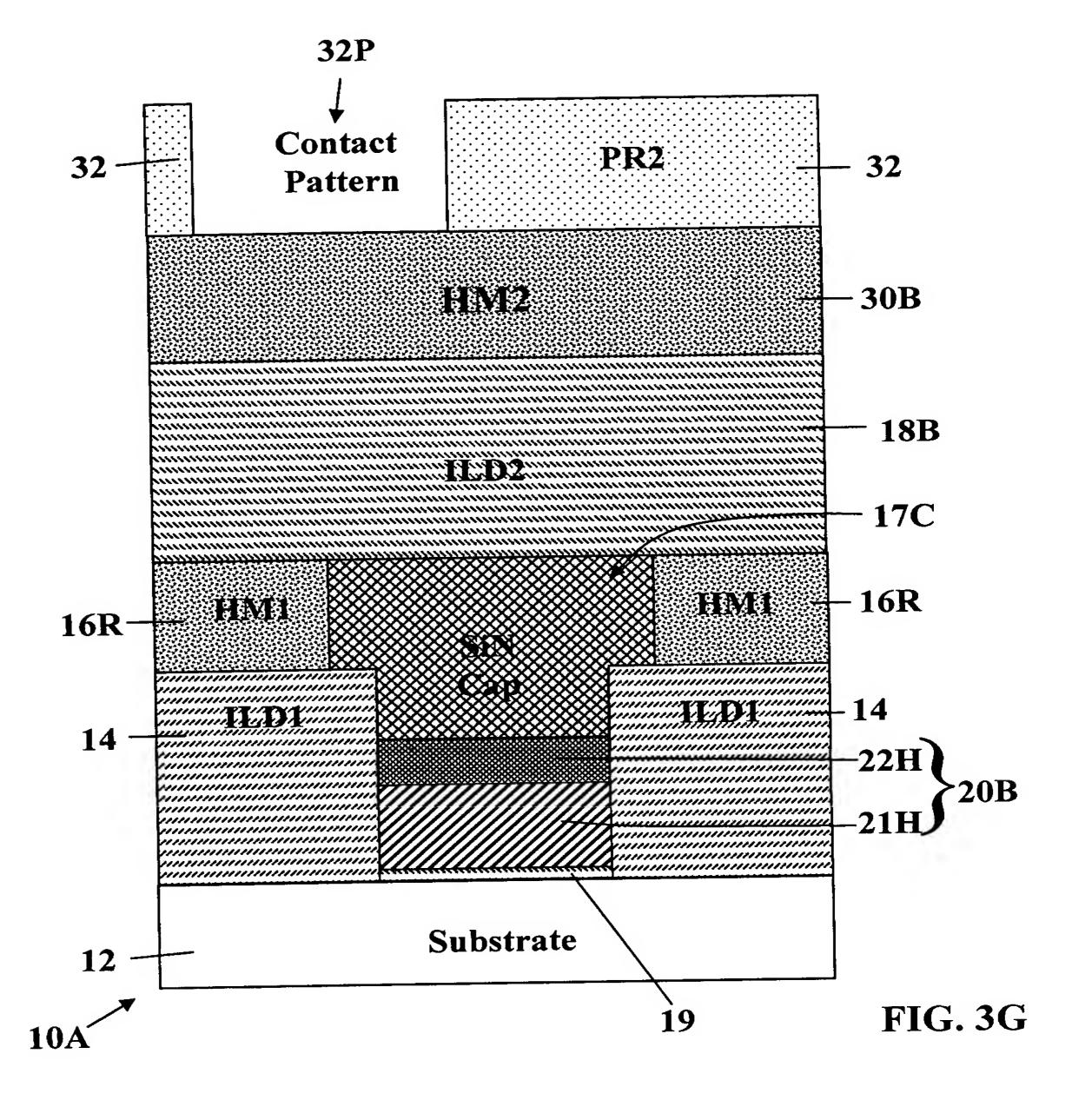
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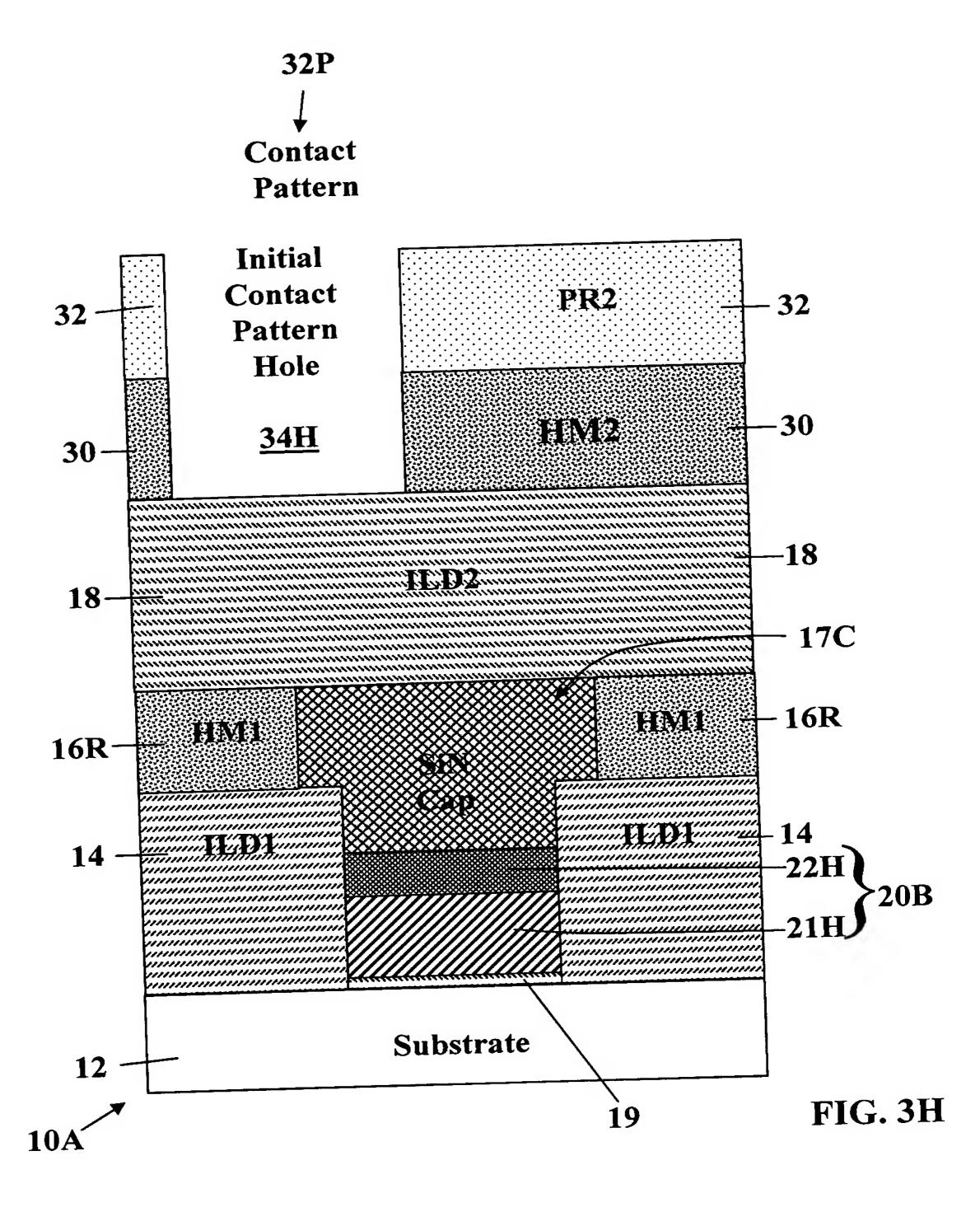


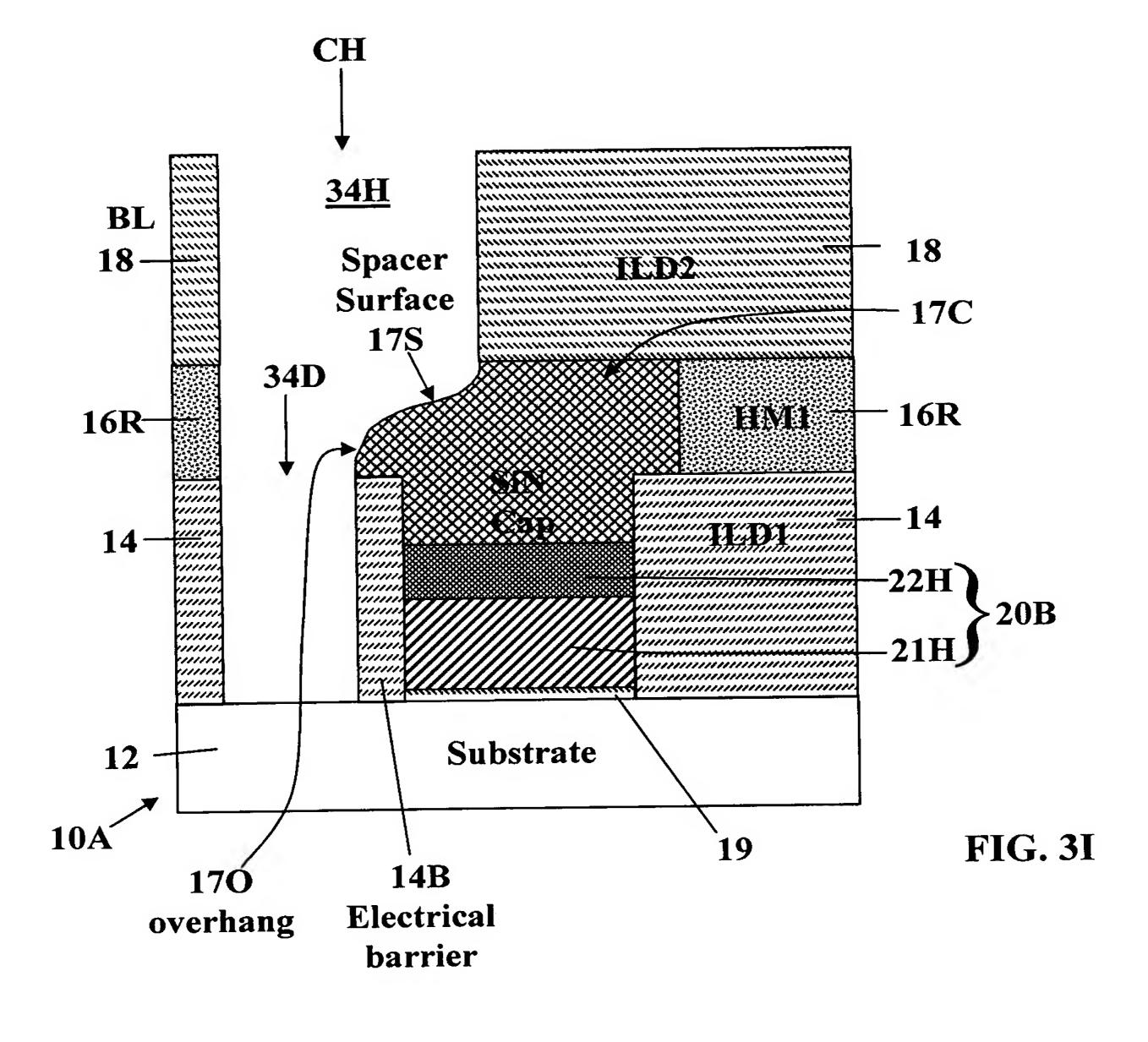


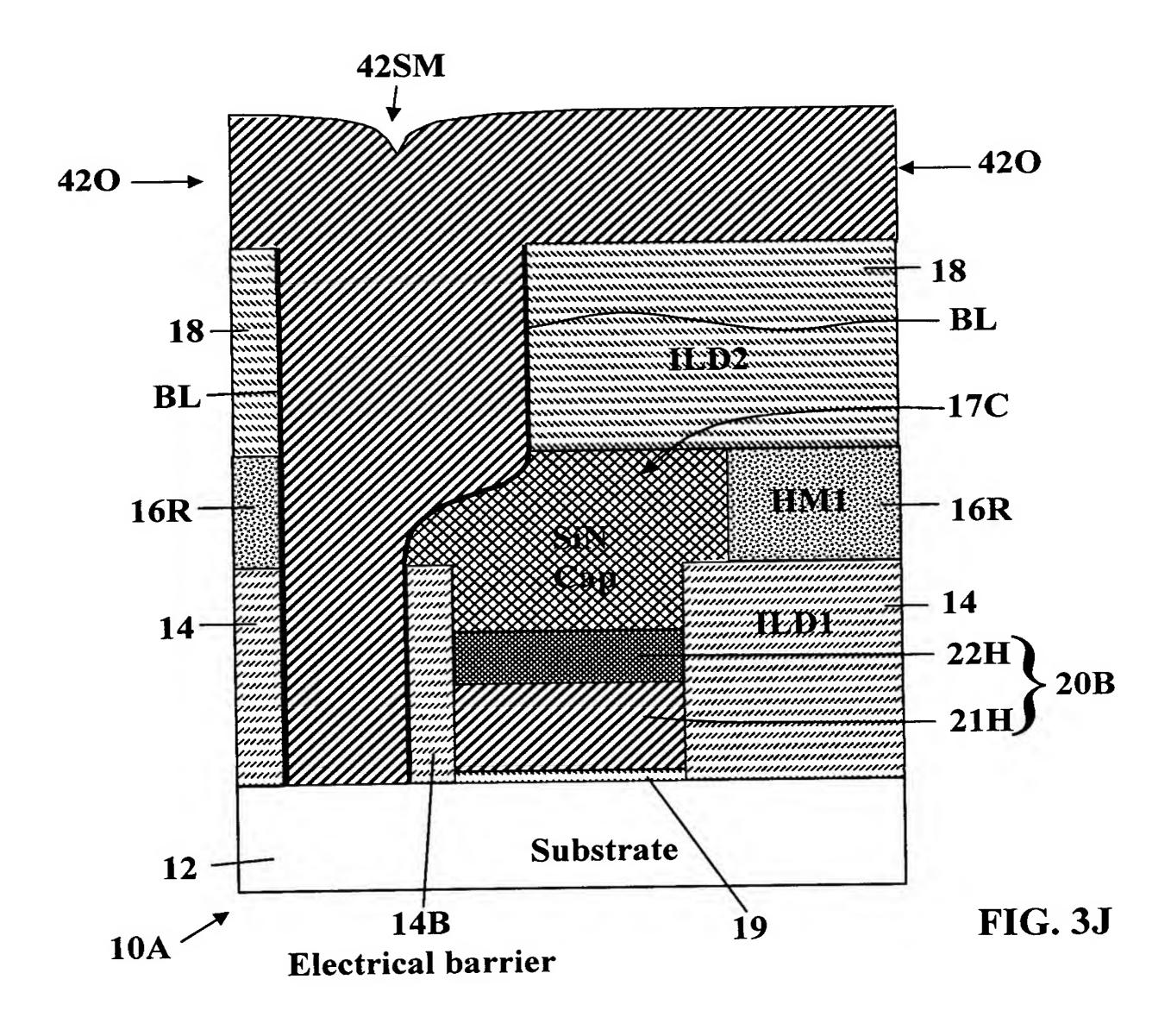


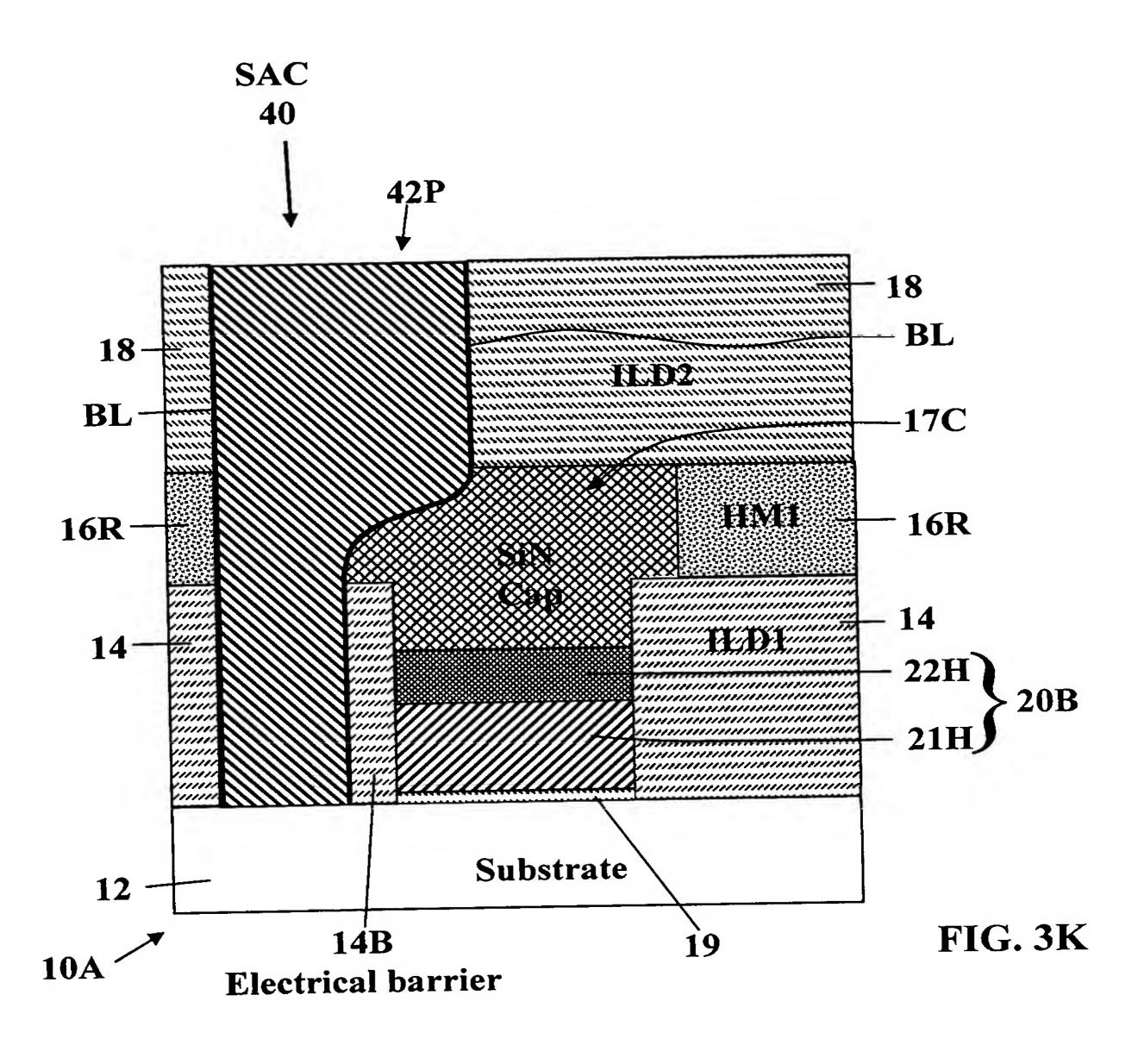












21/26 **START** · **50** · **51** DEPOSIT ILD1 LAYER AND HARD MASK 1 LAYER ON SUBSTRATE 52 FORM PATTERNED RESIST MASK 1 OVER HARD MASK 1 LAYER ETCH MASK 1 PATTERN THROUGH HARD MASK 1 LAYER AND ILD1 · **53** LAYER TO FORM A SLOT DOWN TO OR NEAR SUBSTRATE - 54 STRIP RESIST AND FORM DIELECTRIC ON SUBSTRATE IN SLOT DEPOSIT POLYSILICON ONTO DEVICE AND INTO SLOT. 55' THEN ETCH BACK POLYSILICON TO RECESS IT IN SLOT - 56' FORM RECESSED SILICIDE OVER RECESSED POLYSILICON USE ISOTROPIC ETCH OF HARD MASK 1 TO WIDEN SLOT AT TOP · 57 58 **DEPOSIT CAPPING LAYER 59** PLANARIZE CAPPING LAYER TO EXPOSE TOP OF HARD MASK **60** DEPOSIT ILD2 LAYER AND HARD MASK 2 LAYER ON SUBSTRATE 61 FORM PATTERNED RESIST MASK 2 OVER HARD MASK 2 LAYER ETCH MASK 2 PATTERN THROUGH HARD MASK 2 LAYER AND ILD2 **62** LAYER TO FORM INITIAL CONTACT HOLE PATTERN; STRIP RESIST ETCH SAC CONTACT HOLE THROUGH ILD2, HARD MASK 2 AND ILD1 63 TO SUBSTRATE AND PATTERN SPACER/OVERHANG OF CAP 64 **STRIP HARD MASK 2** DEPOSIT CONTACT MATERIAL IN CONTACT HOLE AND PLANARIZE 65 FIG. 4 66 **END**

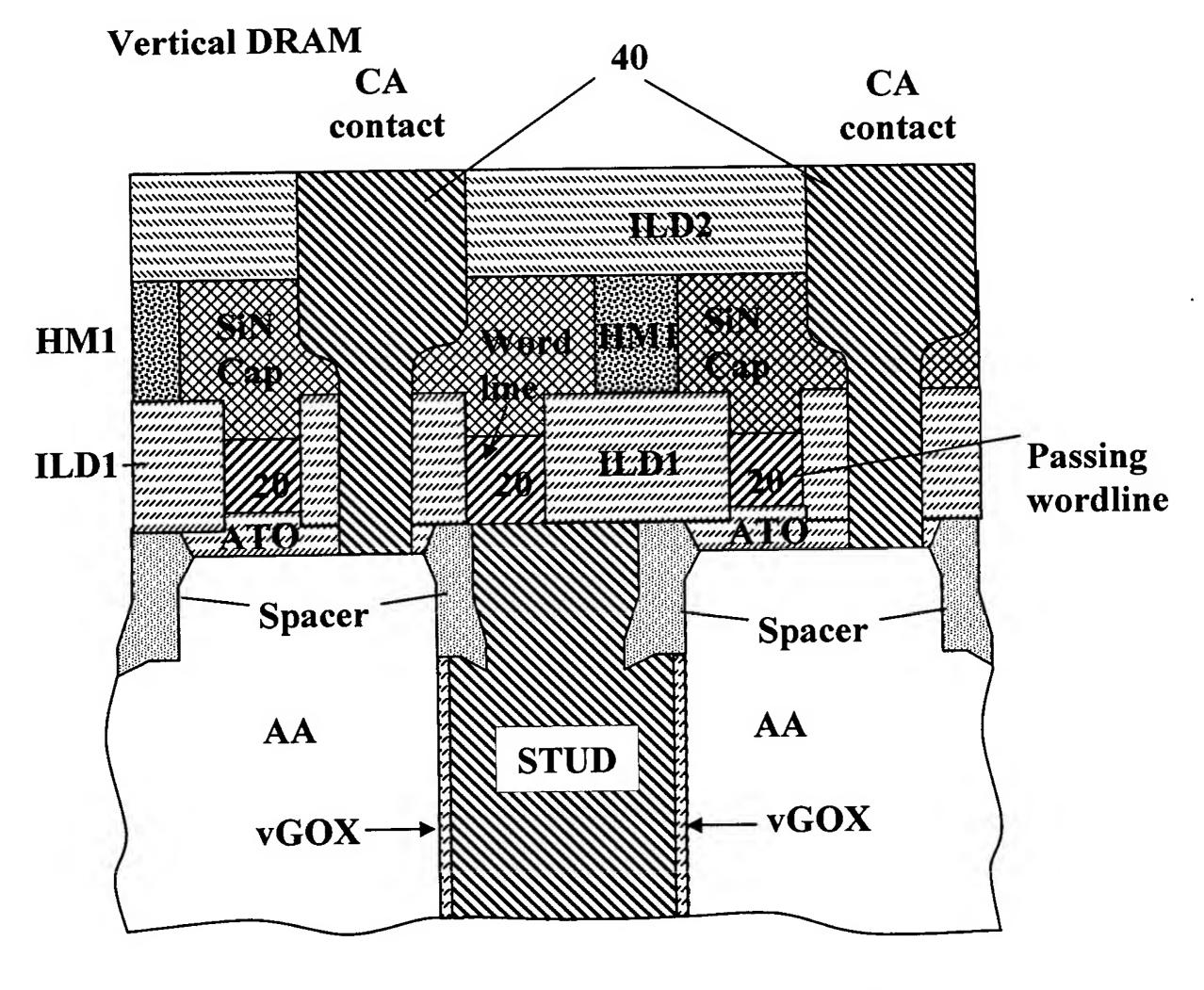
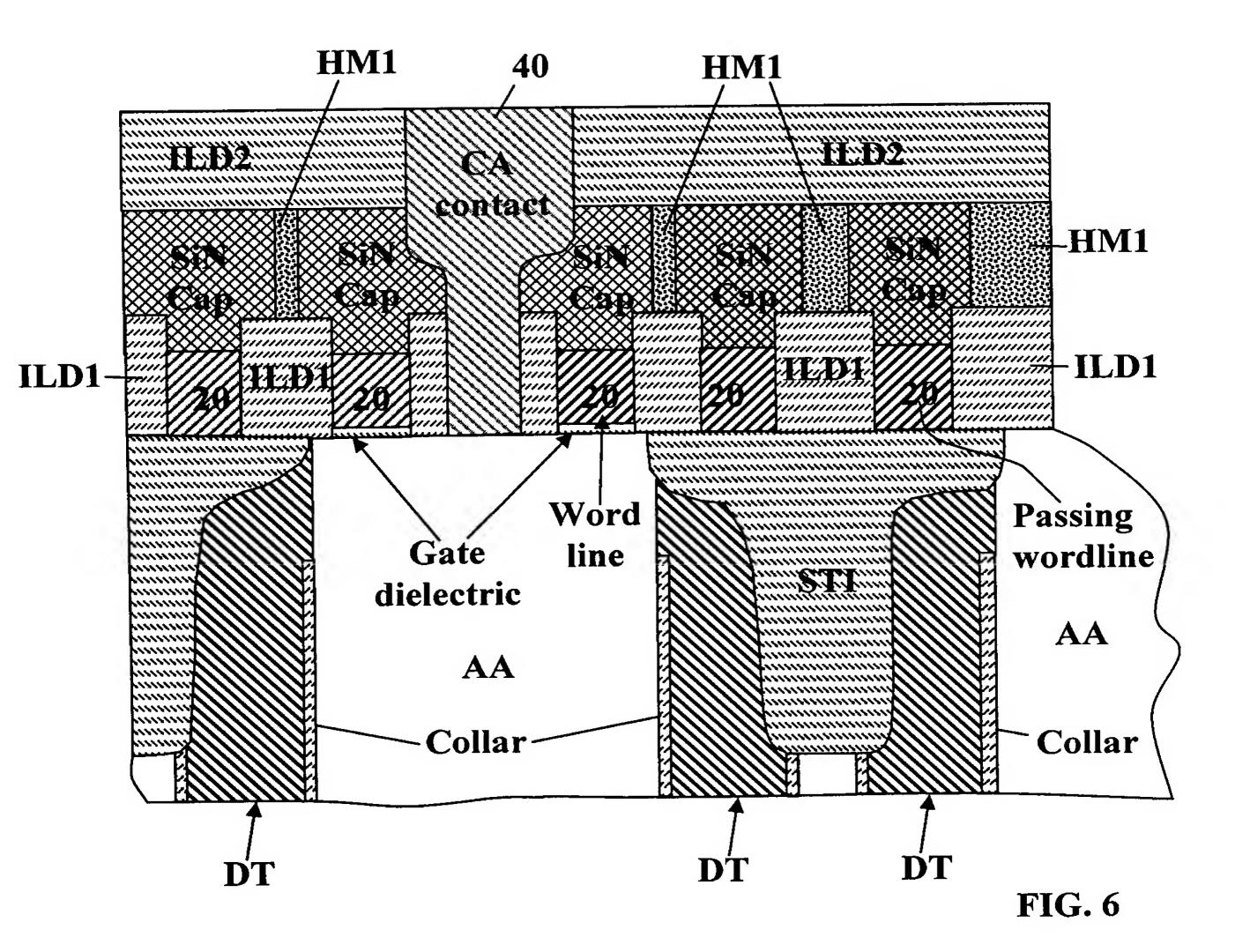


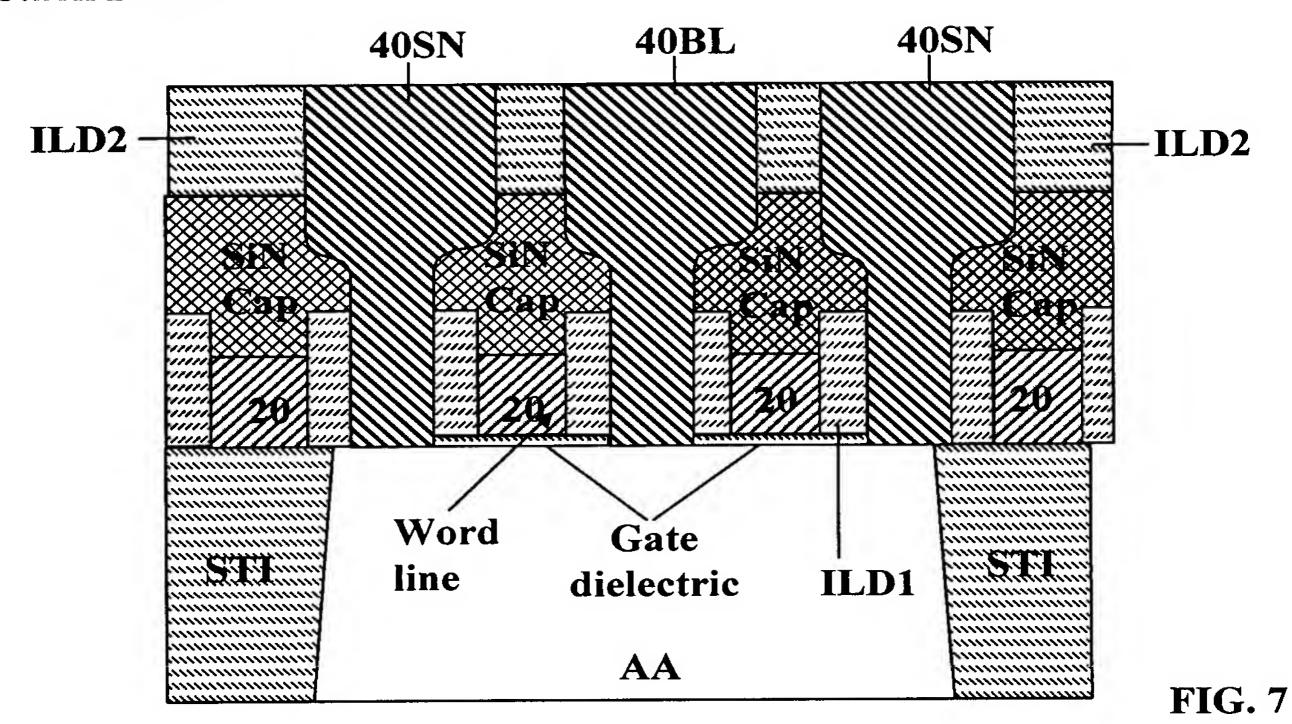
FIG. 5

Planar DRAM



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Stack DRAM



Metal Gate or SRAM

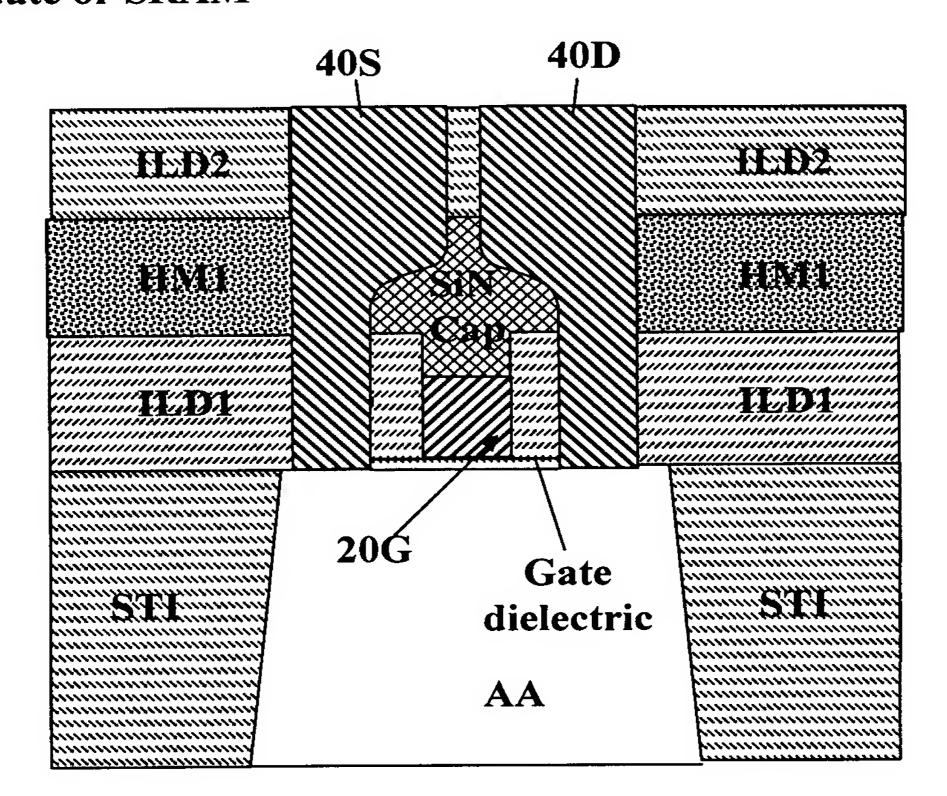


FIG. 8

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Capacitor contact over bit line for stack DRAM

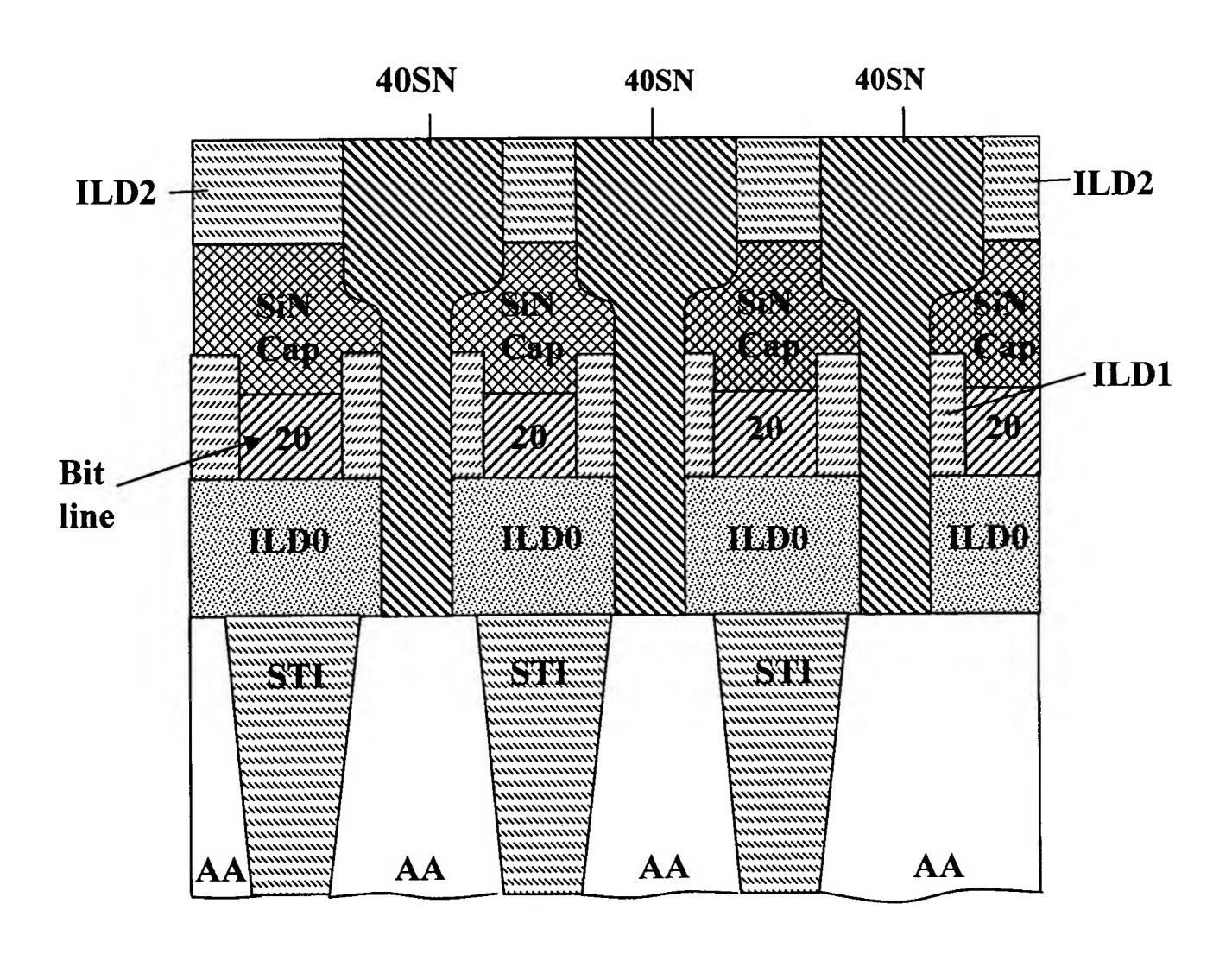
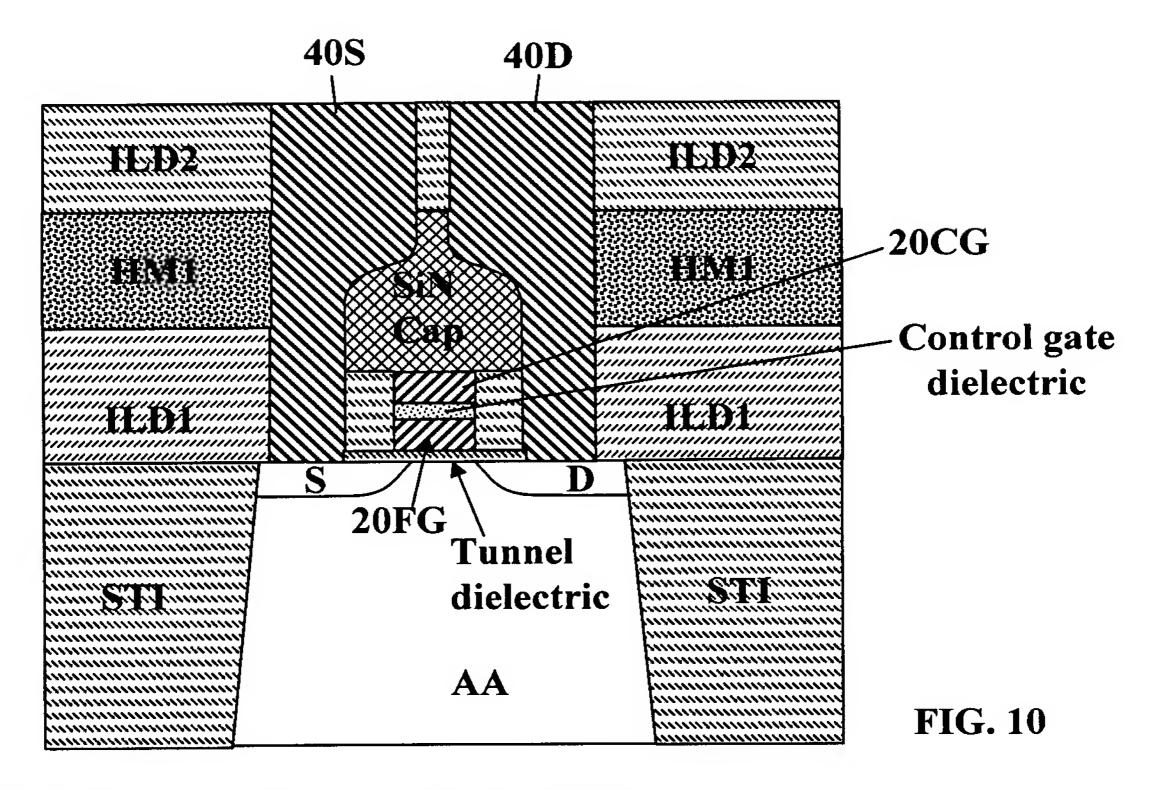


FIG. 9

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High Density Interconnect Line for BEOL

